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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/016,449
Filing Date: December 10, 2001
Appellant(s): BAILIS ET AL.

Kelvin M. Vivian, Reg. No. 53,727

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/30/2006 appealing from the Office action mailed 04/27/20206.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6829751	Shen et al.	12-07-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, 12, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US-6829751), hereinafter Shen.

Claim 1:

Shen teaches a standard cell, the standard cell (Fig. 2, circuit 102) including a plurality of logic functions (Fig. 2, circuit 110, 112, 114); at least one bus coupled to at least a portion of the logic functions; a plurality of internal signals from the plurality of logic functions (Fig. 2, bus and internal signals 140, 142, 144, 146); and a field programmable gate array (FPGA) function (Fig. 2, FPGA Core) coupled to the at least

one bus (Fig. 2, bus 140, 142, 144, 146, 152) and the plurality of internal signals, the FPGA function including a debug client function that observes and manipulates (Col. 2. ll. 39-44, col. 4, ll. 22-24, col. 5, ll. 1-4, col. 6, ll. 21-25, 45-56) the at least one bus and the plurality of internal signals. (Col. 2, l. 39 to col. 6, l. 65). Shen teaches storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server. (Fig. 2, chip registers 120*a*-120*n* and 122*a*-122*n*, Col. 3, ll. 37-41, col. 4, ll. 34-58, col. 5, ll. 36-41).

Shen does not explicitly teach "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server". However, Shen does teach monitoring the correctness of a bus protocol (Col. 6, l. 14), that the FPGA core 116 can also be used to add or verify bug fixes (Col. 6, ll. 52-54), and in claim 1, is configured to detect errors when in a first mode and verifies fixes of errors in said functional portion. It would have been obvious to one of ordinary skill in the art at the time the invention was made to that Shen possesses the claimed comparator logic. The artisan would be motivated to do so because the functions of monitoring, verifying bug fixes, and detecting errors cannot be accomplished without "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server (expected values)". The artisan would also be motivated to do so because in order to verify or detect errors one of ordinary skill in the art must compare (i.e. comparator logic) a result to a known good or expected value.

Claim 9:

Shen teaches a debug client function within an application specific integrated circuit (ASIC, the debug client function being within a field programmable gate array (FPGA) function as per the rejection of claim 1. Shen also teaches the client debug function comprises an external communicator logic function for receiving and transmitting information concerning a plurality of internal signals of the ASIC to a server, selector logic coupled to a plurality of internal signals that are internal to the ASIC (Fig. 2, mux 134, Col. 3, l. 58 to col. 4, l. 3). Shen teaches storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for alter retrieval by the server. (Fig. 2, chip registers 120*a*-120*n* and 122*a*-122*n*, Col. 3, ll. 37-41, col. 4, ll. 34-58, col. 5, ll. 36-41).

Shen does not explicitly teach "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server". However, Shen does teach monitoring the correctness of a bus protocol (Col. 6, l. 14), that the FPGA core 116 can also be used to add or verify bug fixes (Col. 6, ll. 52-54), and in claim 1, is configured to detect errors when in a first mode and verifies fixes of errors in said functional portion. It would have been obvious to one of ordinary skill in the art at the time the invention was made to that Shen possesses the claimed comparator logic. The artisan would be motivated to do so because the functions of monitoring, verifying bug fixes, and detecting errors cannot be accomplished without "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded

from a server (expected values)". The artisan would also be motivated to do so because in order to verify or detect errors one of ordinary skill in the art must compare (i.e. comparator logic) a result to a known good or expected value.

Claim 2:

Shen teaches at least one bus comprises an internal bus (Fig. 2, buses 140, 142, 144, 146).

Claim 3:

Shen teaches the server comprises a debugger server running a debugger application. (Col. 5, ll. 13-25, 41-45, col. 6, ll. 1-17).

Claims 4 and 12:

Shen teaches debug client function (FPGA Core 116) is programmed by a server (Debugging Workstation 104). (Col. 3, ll. 49-54).

Claim 5:

Shen teaches "the debug client function (FPGA core 116) further includes an external communicator logic function for receiving and transmitting information to a server (Debugging Workstation 104)" (Col. 3, ll. 25-26, col. 5, ll. 13-20), and "selector logic coupled to the at least one bus and the plurality of internal signals...", (Fig. 2, mux 134, Col. 3, l. 58 to col. 4, l. 3). Shen also teaches "an interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween" in that there is circuitry within the FPGA core 116 programmed by the Debugging Workstation 104 (Col. 5, 13-25) to execute debugging diagnostics, some of

which are outlined in col. 6, ll. 1-57.

Claim 6:

Shen teaches that the interface logic comprises of a storage logic function for storing a state of signals of interest from the selector logic and providing the state to a server (on chip registers, col. 5, ll. 36-39), a comparator logic function coupled to the storage logic function for comparing the signals of interest from the selector block function (Col. 5, ll. 39-45, col. 6, ll. 32-44), and an output logic function coupled to the comparator logic function for controlling the internal signals on the ASIC (Col. 3, ll. 22-27, ll. 49-54).

Claims 7 and 14:

Shen teaches the server utilizes the debug client to debug hardware within at least one of the plurality of logic functions. (Col. 2, ll. 42-45, Fig. 2).

Claims 8 and 15:

Shen teaches the server utilizes the debug client to debug software within at least one of the plurality of logic functions. (Col. 6, ll. 1-63).

(10) Response to Argument

Whether or not Claims 1-9, 12, and 14-15 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen.

The Appellants argues on **pages 4-6, section (A)(i)**, "Shen fails to disclose an FPGA having a debug client function that includes comparator logic operable to

compare selected ones of a plurality of internal signals coupled to the FPGA with a trigger pattern downloaded from a server". The Examiner agrees that Shen does not explicitly teach a debug client included in the FPGA includes "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server". However, the Examiner asserts that Shen does teach that the FPGA core 116 programmed by the debug software from the debugging workstation 104 includes monitoring the correctness of a bus protocol (Col. 6, ll. 1-4, 14), that the FPGA core 116 can also be used to add or verify bug fixes (Col. 6, ll. 52-54), and in claim 1, is configured to detect errors when in a first mode and verifies fixes of errors in said functional portion. The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to that Shen possesses the claimed comparator logic. The artisan would be motivated to do so because the functions of monitoring, verifying bug fixes, and detecting errors cannot be accomplished without "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server (expected values)". The artisan would also be motivated to do so because in order to verify or detect errors one of ordinary skill in the art must compare (i.e. comparator logic) a result to a known good or expected value. By this the Examiner asserts that Shen does not "teach away" from including comparator logic within the FPGA, as the Appellants contends (see arguments page 5, third paragraph), but fully supports the notion.

The Appellants also argues on **page 5, second paragraph**, "While Shen discloses performing the functions of monitoring, verifying bug fixes, and detecting errors, Applicant submits that these functions are performed by the debugging workstation (or circuit) 104 (working with the FPGA core 106), which debugging workstation 104 is not contained within the FPGA core 102 (see col. 2, ll. 63-65; FIG. 1). That is, Shen discloses that data is collected from the FPGA core 106 and sent to the debugging workstation where the internal signals are analyzed (col. 3, ll. 52-57; col. 4, ll. 55-58)". The Examiner asserts that indeed the FPGA core 116 performs the functions of monitoring, verifying bug fixes, and detecting errors, not the debugging workstation 104 as the Appellant purports. In the Abstract Shen discloses a system for designing an integrated circuit (IC), where this system comprises a circuit and a programmable portion (the FPGA core 116) **used for diagnostics and finding bugs**. The programmable portion (the FPGA core 116) may be configured (i.e. by the debugging workstation 104, see col. 4, ll. 36-37) **to detect, correct and/or diagnose errors in the logic portion through the one or more interfaces**. This also supports the rejection of the limitation "the debug client function being in communication with a server" of claims 1 and 9. Also, in column 2, ll. 41-45, Shen teaches "[t]he FPGA core can be used to implement on-chip diagnostics to enable debugging functions, such as bus monitoring, probing, single step running, triggering, capturing, etc.". Further, Shen teaches "[t]he system 100 may provide a chip diagnostics architecture by implementing the FPGA core 116. By using the FPGA core 116 to implement such chip diagnostics, simultaneous probing of internal signals can be achieved...". (Col. 3, ll. 32-35). Again,

"users can also program the FPGA core 116 to implement different debugging functions. (Col. 5, ll. 41-45). These functions are disclosed in column 6, lines 1-17, 31-56). The Appellants attempts to strengthen their position by arguing, "Shen discloses that data is collected from the FPGA core 106 and sent to the debugging workstation *where the internal signals are analyzed* (col. 3, ll. 52-57; col. 4, ll. 55-58)". However, the Examiner asserts that Shen never analyzes the transferred data, but only displays the waveforms of the signals. In fact, Appellants assertion "*where the internal signals are analyzed*" is never stated in the cited col. 4, ll. 55-58, but added by the Appellants. Shen discloses in column 3, lines 52-57 (cited by the Appellants) "[a]fter the data is collected and compressed (by FPGA 116), the data will be sent to the debugging workstation 104. The waveforms of the internal signals under probing **can be displayed** as if they are directly connected to a logic analyzer by internal wires (via the debugging workstation 104). The compressed data is not analyzed by the debugging workstation 104 at all, but merely displayed.

By the arguments presented above the Examiner has shown, in no uncertain terms, to one skilled in the art that Shen's FPGA core 116 does indeed include comparator logic and the debugging function as claimed.

The Appellants argues on **page 6, section (A)(ii)**, "Shen fails to disclose an FPGA having storage logic operable to store a state of selected ones of a plurality of internal signals that matches the trigger pattern for later retrieval by a server". To support this argument the Appellants argue "Shen discloses storing only signals within the FPGA core 116 that are pre-selected by a user, and not signals that match a trigger

pattern". The Examiner disagrees and asserts that Shen teaches the claimed "storage logic (**Fig. 2, register blocks 120a-120n and 122a-122n, FPGA core 116 probes internal signals**, Col. 3, ll. 32-42, 49-51, col. 4, ll. 4-11) operable to store a state of selected ones of a plurality of internal signals (**user can decide which signals need to be observed**, col. 5, ll. 31-32) that matches the trigger pattern (**programming the FPGA core 116 to implement user required functions**, col. 5, ll. 17-18 and **debugging features of the FPGA core 116**, col. 6, ll. 1-17) for later retrieval by a server (**the FPGA core 116 transfers the selected ones of a plurality of internal signals back to the debugging workstation 104**, col., ll. 55-58)". The Examiner's claim interpretation is further supported by the Appellants' disclosure on page 6, lines 10-14, which reads "[t]he stateful and stateless comparators and client control logic function block 126 is the logic that compares the signals of interest (claimed "selected ones of a plurality of internal signals") with the "trigger" pattern that is down-loaded from the debugger server and upon a match, directs the signal and bus state storage logic function block 124 to store the signals of interest. In other words, a user pre-selects the "signals of interest" (the selected internal signals) by programming the FPGA from the debugger workstation and stores those signals of interests (i.e. the pre-selected internal signals) in the FPGA. Therefore, the Examiner asserts that Shen teaches all aspects of the argued limitations.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

John J. Tabone, Jr. 11/06/2006

Conferees:

Kim Vu (SPE)

Shelly Chase (Primary Examiner)